

Sam L. Rainwater

EDUCATION:

BSEE, Cal State Univ. Northridge, 1976, Magna Cum Laude

AS, Los Angeles Pierce Jr. College, 1973, President's Award

Other Education/Industry Training:

Communications Courses, National Radio Institute, Graduate with Honors

Radiation Effects on Electronics

Radio and Carrier Communications

Microwave Communications

Transistor Equipment

Various Management Courses

IEEE NSREC Short Courses 1985 through 2010

WORK SUMMARY:

YEARS OF PROFESSIONAL EXPERIENCE: 30+YRS

AS OF : July 2015

Thirty + years R & D experience including hardened subsystems, power supplies, precision analog, servos, radio/laser communications, non-volatile memory, computer systems, and test equipment. Program experience includes: Power subsystems for P321, GPSIII, SBIRS, AEHF, Responsive Space, EOS, F11, GPSII, Milstar II spacecraft, space solar/battery, Space Station Communications Power, Super Space Power, MSX Sensor Satellite, DSP Thermal Control System, F-16 IFF & MLS; Memories for B-1, B-2, F-15, F-18, Small ICBM and ALCM/GLCM/Tomahawk Cruise Missile Computers; Cruise Missile Radiation Detectors and Circumvention Mechanization, Seeker/Sensor AGT instrumentation, Fast Hunters Trophy AGT & UGT LWIR instrumentation, Delta 180 digital laser loop control system, and various communications programs. Power supply experience includes most major Topologies including; Forward converter, Boost, Buck, Flyback, SEPIC and Mag-Amp. Radiation test experience includes Brookhaven, Texas A&M, Livermore and Indiana University Cyclotrons, SAIC CXR, TRW Vulcan SFXR, Boeing Dynamitron, Little Mountain LINAC and FXR, WSMR FBR and LINAC, TITAN 1150, Double Eagle and Python, NPGS FXR, Maxwell Laboratories Blackjack 3, Phillips Laboratories Febetron and Co60, and NTS UGT. Sam has been involved with FDM, TDM, PPM, PDBM, and PQM communications, ranging from 10 BPS to 1GBPS and HF to 0.53 uM laser carriers. He has held memory design responsibility in NDRO and DRO Core, Bipolar, CMOS, Silicon Nitride, Disk and Bubble technologies with various circumvention system designs. Circuit Experience includes Power Circuitry, Interface, A/D, D/A, Memory Peripherals, Logic, Memory Systems, Microprocessors, Discrete Amplifiers (DC to VHF), Op Amps, Switching Regulators, High Speed Current Sources, Pulse Transformers, Delay Lines, Sense Amplifiers, and Radiation Hardened Digitals/Linears. Skills include electrical and radiation design, analysis, laboratory testing, qualification tests, reliability prediction and product quality assurance testing/hardness assurance, management of products, departments and development organizations. Technical writing skills are excellent. Has written many winning proposals for major developments and has submitted a multitude of "first time acceptance" support documents and analysis. Has 3 patents and has presented/contributed on numerous papers for industry conferences and journals.

PROFESSIONAL EXPERIENCE:

09/87 - Present: Consultant/Consulting Employee, Various Corporations

Presently as part owner of Suntronics and for the past 26 years, Sam has provided support to clients in all areas of circuit design and analysis including Survivability design, System design, Analog Circuit Design, non-volatile memory design, switching power sub-system design, Reliability Engineering and NH&S. Current and Recent/Current program support includes GPSIII, SBIRS, AEHF, GOES-R, D5 Life Extension, Irridium Next, Various NH&S testing programs, numerous Worst Case analysis, power supply designs, analog instrumentation, portable instrument and on going proposal activities.

01/80 - 09/87 Vice President of Engineering, QUADRI CORPORATION

Chief Engineer responsible for research, development and production support of a variety of non-volatile memory products, power supplies and test equipment. He managed development of the Small ICBM NDRO Core Hardened RAM, RMW Core Memory Product Lines (Q65, QT, AC and Q32), and hardened satellite power subsystems. Personal contributions included

design of the Small ICBM WCS bubble memory study, radiation analysis and testing at WSMR, Little mountain, Boeing and SAIC. Responsibilities included design and management of engineering personnel, assets, subcontractors, consultants, and marketing support.

/78 - 1/80 Project/Task Leader, MOTOROLA GED

Laser Communications tracking computers, communication modulators, and other electronic systems design on fast turn around programs: an 8 month Control Computer with Bit Slice Processors, Precision Analog I/O and High Speed Signal Conditioning; a 12 month space experiment utilizing uP, Precision Analog I/O, High Speed Signal Conditioning and Intelligent command/Telemetry (subsequently utilized on Delta 180 experiment); and a 27 day space flight qualified VHF Phase Lock Loop.

6/74 - 1/78 Memory Systems Design Engineer, Litton Guidance & Control

Military semiconductor and core memory responsibility including complete electrical design, nuclear design, analysis and test, characterization mechanical/thermal interfaces, design review presentation, cost estimating, proposals, vendor specifications, reliability predictions, test equipment design, and production engineering support. Program experience included hardened guidance computers for Cruise Missiles from design/qualifications through hardness assurance in production.

6/73 - 6/74 Production System Technician, SINGER LIBRASCOPE

Responsible for troubleshooting and test of production fixed head Magnetic Disk Memories.

7/70 - 6/73 Shop Supervisor/Radio Technician, HENRY RADIO, INC

Responsible for supervision of Amateur Radio equipment returned for repair and the troubleshooting, repair and test of said equipment.

3/65 - 7-70 Electronic Technician, UNITED STATES ARMY

Various responsibilities from operation of radar equipment to depot level maintenance of telecommunications equipment. (Obtained highest rating in U.S. Army in job classification during last year of service.) Platoon sergeant for communications platoon in Viet Nam (Microwave).

SECURITY CLEARANCE:

I currently hold a DoD Secret.

COMPUTER PROFICIENCY:

Language/Tools: P-Spice 8 & 9, IsSpice, MathCad, Relex, MS Word, Excel, Word Perfect, Lotus, MacDraw, PageMaker, Power Point, Harvard Graphics, Corel, MS Project & Various other Program Management Tools, Fortran, Basic.

Hardware Systems: IBM PC's & Compatibles, Macintosh

Operating Systems: MS-DOS, WindowsXX, Macintosh

MISCELLANEOUS:

Honoraries: Tau Beta Pi

Licenses: 1st Class Radio Telephone, Amateur Radio Operator

Member of IEEE, MENSA

CUSTOMERS:

NORTHROP-GRUMMAN, LOCKHEED MARTIN, BOEING, LORAL, GE, MARTIN, JPL, APL, VPT, SINGER, DSWA, NASA, USAF-BMO, USA-SDIO, USAF-AFRL, NRL, NSC

SKILLS SUMMARY:

Electronic Engineering, Power Converter Engineering, Analog Design Engineering, Computer H/W Engineering, Reliability Engineering, Environmental Engineering, Survivability Engineering, Radiation Hardening, Program Management, Project Management, Task Management, Technical Writer, Technical Editor

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Papers & Presentations

"Power Supply Dose Rate Hardening Seminar". Raytheon, El Segundo, February 1999

"Interceptor Sensor Ensemble Survivability Test Protocol Demonstration" with others, 99 HEART, March 99, Monterey Ca

"FAST Program Results: An Evaluation of the Correlation of the AGT/UGT Test Results and Implications for Sensor System Testing" with others. 1994 HEART, Feb 94, Monterey Ca

"Design Guidelines for a Nuclear Hardened and Low Noise Operation Infrared Assembly" with others. 1994 HEART, Feb 94, Monterey Ca

"LWIR FPA FXR Test in the Hardened FAST Assembly" with John Retzler. 1994 HEART, Feb 94, Monterey Ca

"LWIR Si:As Detector High Prompt Dose Testing Terminal Protection Unit and Combined FXR/CIT" with John Retzler. 1993 HEART, Feb 93, Orlando Fl

"LWIR Detector Array Enhanced Gamma and Neutron Testing" with John Retzler. 1993 HEART, Feb 93, Orlando Fl

"Above Ground and Under Ground Testing of a Hardened State-of-the-Art LWIR FPA Assembly - Double Eagle and Hunters Trophy" with others. 1993 HEART, Feb 93, Orlando Fl

"FAST Program UGT/AGT Data and Hardware Review" with others. 1993 HEART, Feb 93, Orlando Fl

"GaAs Solar Cell Array Flash X-Ray Response, with John Retzler and others. 1991 RHETC, Oct 91, Rockwell Intl, Anaheim Ca

"A rechargeable Solid State Energy Source for use with Hardened SRAM's" with John Bruder. 1991 NVMT, June 91, Baltimore Md

"Circumvention Hardened Field Effect Transistors" with others. 1990 GOMAC, Nov 90, Las Vegas Nev

"Miniaturization of NDRO Core Technology", with John Bruder. 1990 RHETC, Oct 90, A.F. Academy, Co Springs Co

"Smart Power Circumvention Development" with others. 1990 RADIATION HARDENED LINEAR IC WORKSHOP, May 90, Tucson Az

"Smart Power Circumvention Development for Non-Developmental Items" with others. 1989 SAIC REPORT, Nov 17, 89 - SAIC/89-1637

"Smart Power Circumvention Development" with others. 1989 GOMAC, Oct 89, Orlando Fl

"NDI Circumvention", with John Retzler, Journal of Radiation Effects, Research and Engineering Vol 8-2A Pg37 . 1989 HEART, Feb 89, Melbourne Fl

"SGEMP Character of a Magnetic Core Memory, with Morrison, and others. 1988 HEART, Feb 88, El Toro NAS, Santa Ana Ca -

"NDI/INR Circumvention Final Report" with others. 1988 SAIC REPORT, Jan 88

"SEU Fault Tolerant Magnetic Memories" with John Retzler. 1987 IEEE NSREC, July 87, Snowmass Co

"Bubble System Architecture" with Sam Baker. 1987 NVMT, June 87, Baltimore Md

"Hardening of Core Memories" with Sam Baker. 1987 NVMT, June 87, Baltimore Md

"SEU Fault Tolerant Magnetic Memories" with John Retzler. 1987 SYMPOSIUM ON SINGLE EVENT EFFECTS, April 87, Los Angeles Ca

"Core Memory Test Results" with John Retzler. 1986 RHETC, October 86, Melbourne Fl

"Core Memory SGEMP Response" with Ron Weitz. 1986 HEART, Jul 86, Naval War College, Newport RI

"NDRO Core Memory Simulation Using RADSPICE™ with others, IEEE Trans. Nuc Science Vol NS-33, No 6, Dec 86. 1986 IEEE NSREC, July 86, Newport RI

"The vulnerability of the Pershing II Missile to Particle Beam Weapons" with others, SAIC-102-85-022. 1985 SAIC REPORT, Dec 85

"Neutral Particle Beam Effects on Missile Electronics" with others, Journal of Radiation Effects, Research and Engineering Vol 4 No. 1, 1984. 1985 HEART, July 85

"LCM9000 Hard Core Memory" with John Retzler. 1980 RHETC, Nov 80, Clearwater Fl

"AGM-86 Nuclear Hardness Assessment Report" with others, 5 Volumes, 7 appendices, Litton G&CS 403498. 1980 LITTON REPORT, 1978-1980

"AGM-109 Nuclear Hardness Assessment Report" with others, 5 Volumes, 7 appendices, Litton G&CS 403576. 1980 LITTON REPORT, 1978-1980

"AGM-86 Radiation Test Report" with others, 2 Volumes, 13 appendices, Litton G&CS 403499. 1980 LITTON REPORT, 1978-1980,

"AGM-109 Radiation Test Report" with others, 2 Volumes, 13 appendices, Litton G&CS 403578. 1980 LITTON REPORT, 1978-1980,

Patents

Patent number: **4965828**

Non-volatile semiconductor memory with SCRAM hold cycle prior to SCRAM-to-E.sup.2 PROM backup transfer

Patent number: **4805146**

Soft write apparatus and method for nondestructive readout core memory

Patent number: **4965828**

Non-volatile semiconductor memory with SCRAM hold cycle prior to SCRAM-to-E.sup.2 PROM backup transfer